What is claimed is:

1. An analog delay locked loop device comprising:

a first block for receiving an internal clock signal and a reference clock signal to generate normal multi phase clock signal pairs and dummy multi phase clock signal pairs; and

a second block for receiving the reference clock signal to generate a delay locked internal clock signal having a corrected duty cycle based on the normal multi phase clock signal pairs and the dummy multi phase clock signal pairs.

2. The analog delay locked loop device as recited in claim 1, wherein the first block includes:

a reference delay line which receives the internal clock signal to output the normal multi phase clock signal pairs and the dummy multi phase clock signal pairs; and

a reference control means which forms a reference loop with the reference delay line and controls the reference delay line for the reference clock signal and one signal of last clock signal pair of the normal multi clock signal pairs to have a phase difference of 180°.

3. The analog delay locked loop device as recited in claim 1, wherein the second block includes:

a clock interface which selects one of the normal multi phase clock signal pairs and one of the dummy multi phase clock signal pairs from the reference delay line to perform a

duty cycle correction by mixing phases of each signal of the selected normal multi phase clock signal pair and by mixing phases of each signal of the selected dummy multi phase clock signal pair;

a fine delay line which receives outputted signals from the clock interface to output the delay locked internal clock signal;

a delay model for modeling a delaying quantity for the delay locked internal clock signal outputted from the fine delay line;

a fine delaying means for controlling a delaying quantity of the fine delay line by comparing a feed-backed clock signal from the delay model with the reference clock signal;

a control means which receives the reference clock signal and the feed-backed clock signal to control the clock interface; and

a duty correction amplifying means for supporting the clock interface to correct duty cycle ratio receiving outputted signal from the fine delay line.

4. The analog delay locked loop device as recited in claim 2, wherein the reference delay line includes:

a normal delay line which receives the internal clock signal and has a plurality of serial connected differential delay cells for generating the normal multi phase clock signal pairs; and

a dummy delay line which receives the last clock signal pair from the normal delay line and has a plurality number of serial connected differential delay cells.

5. The analog delay locked loop device as recited in claim 3, wherein the clock interface includes:

a phase multiplexing means controlled by the control means to select one of the normal phase clock signal pairs and one of the dummy phase clock signal pairs from the reference delay line; and

a phase mixing means for mixing phases of the selected normal phase clock signal pair and for mixing phases of the selected dummy phase clock signal pair.

6. The analog delay locked loop device as recited in claim 5, wherein the phase multiplexing means includes:

a first multiplexer for outputting one of the normal multi phase clock signal pairs in response to a phase selection signal outputted from the control means;

a second multiplexer for outputting one of the dummy multi phase clock signal pairs in response to the phase selection signal;

a third multiplexer for selectively outputting the one of the normal multi phase clock signal pairs from the first multiplexer in response to an even-odd selection signal outputted from the control means; and

a fourth multiplexer for selectively outputting the one

of the dummy multi phase clock signal pairs from the second multiplexer in response to the even-odd selection signal

7. The analog delay locked loop device as recited in claim 5, wherein the phase mixing means includes:

a first source-coupled pair which receives a normal differential clock signal pair and has a first fixed current source;

a second source-coupled pair which receives a dummy differential clock signal pair and has a second fixed current source;

a first load unit connected to the first source-coupled pair and the second source-coupled pair for forming a differential amplifier;

a first differential amplifying unit which receives a duty control voltage outputted from the duty correction amplifying means; and

a bias control unit for controlling a sink current of the first source-coupled pair and the second source-coupled pair by mirroring a differential current outputted from the first differential amplifying unit.

8. The analog delay locked loop device as recited in claim 7, wherein the bias control unit includes:

a first MOS transistor and a second MOS transistor for mirroring the differential current outputted from the first differential amplifying unit;

a third MOS transistor and a fourth MOS transistor which are operated as a current sink for the mirrored differential current;

a fifth MOS transistor and a sixth MOS transistor connected parallel to the first fixed current source and to the second fixed current source respectively to control a bias of the first source-coupled pair and the second source-coupled pair; and

a switch for switching between gates of the third and fourth MOS transistors and gates of the fifth and sixth MOS transistors in response to the bias selection signal outputted from the control means.

9. The analog delay locked loop device as recited in claim 8, wherein the duty correction amplifying means includes:

a second differential amplifying unit which receives an output from the fine delay line;

a first current mirroring unit for mirroring a current outputted from a sub output terminal of the second differential amplifying unit;

a second current mirroring unit for mirroring a current outputted from a main output terminal of the second differential amplifying unit;

a first cascade load and a second cascade load connected between the first current mirroring unit and the second current mirroring unit; and

a first capacitor and a second capacitor for generating the duty control voltage by charging an output current from the first mirroring unit and the second mirroring unit.

10. The analog delay locked loop device as recited in claim 6, wherein each of the first multiplexer and the second multiplexer includes:

a plurality of selection units having a seventh MOS transistor, a first MOS transistor and a second MOS transistor pair; and

a second load unit connected to the selection units,

wherein, a gate of the seventh MOS transistor receives a bias voltage, gates of the first MOS transistor receive the normal multi phase clock signal pairs in the first multiplexer and receives the dummy multi phase clock signal pairs in the second multiplexer, gates of the second MOS transistor receive the phase selection signal.

11. The analog delay locked loop device as recited in claim 9, wherein each capacitance of the first capacitor and the second capacitor has the same capacitance.

12. The analog delay locked loop device as recited in claim 1, wherein the reference clock signal and the internal clock signal are in phase.

13. The analog delay locked loop device as recited in

claim 12, wherein the internal clock signal is used as the reference clock signal.

14. The analog delay locked loop device as recited in claim 2, wherein the reference control means includes:

a phase detector to compare a phase of the reference clock signal with that of the last clock signal pair of the normal multi clock signal pairs;

a charge pump receives an output from the phase detector as its input; and

a loop filter to receive an output from the charge pump having a capacitor.